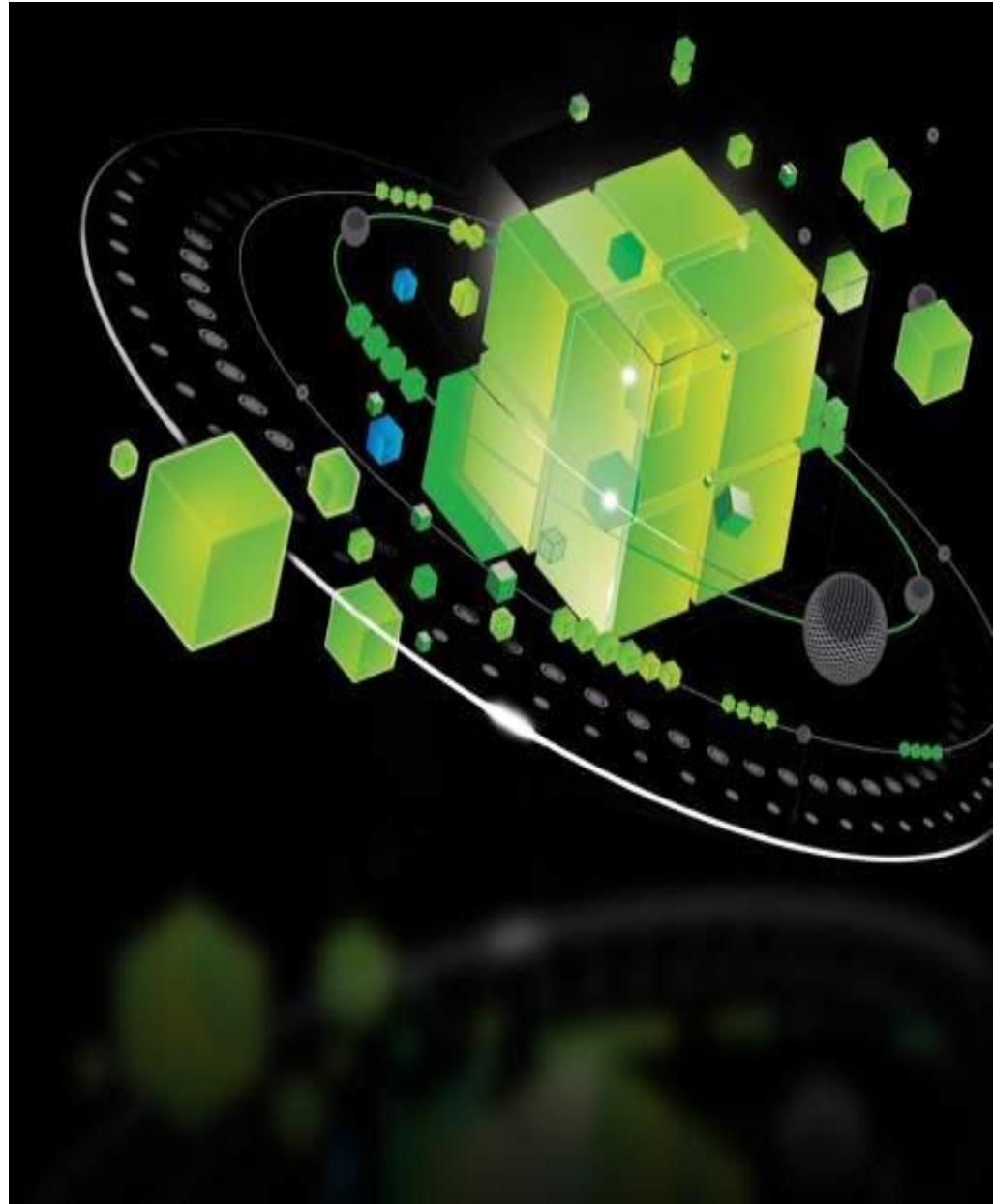


IBM z196 zEnterprise

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Agenda

- **Introduction/Background**
- **Implementation considerations**
- **Hardware feature comparison**
- **Hiperdispatch**
- **Experiences and observations**



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Introduction/Background

George Handera - SE Capacity

Aetna has 2 datacenters - 25 miles apart

14 - 2097's and 1 - 2817

Each datacenter has a pair of external CF CECs

One datacenter has 1 SYSPLEX over 8 CECs - heavy Datasharing over 16 ICB4 links

Second datacenter 6 SYSPLEXES over 6 CECs plus the ESP box
Datasharing load is light over PSIFB and ICB4 links



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- **What's new with the z196**
- Energy attributes
- New level of cache on the CHIP
- New instruction support for C and Java environments
- Vertical scalability - applies to the LPAR as well as the CEC
- Large Page support evolving - benefits Websphere and DB2 workloads
- ETR timing no longer supported, STP implementation requires
- ICB4 links (high speed Coupling Facility links) no longer supported, PSIFB links best option for ICB4 replacement.



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Implementation Considerations

- Cooling - Water option available, our box is Air cooled
- Power - DC option available, our box runs AC
- STP no longer an option – time to get rid of the timer!
We initially established a Mixed-CTN to support the 2817
- PSIFB – While Infiniband is not new, the 2097 was the last machine that supports ICB4 links.

PSIFB becomes the replacement technology on the 2817. Our ESP testing experience focused on PSIFB for the Coupling Facility.



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Feature Comparison Table z9, z10 and z196

Series Model	Number of CPU's	Mips	Max Memory	Chip Cores	Cache Levels	Bus Speed	CPU GHz	CF High Speed Links
Z9 2094	1 - 54	580	512 GB	DUAL	2	2.7 GB	1.7	16-ICB4
Z10 2097	1 - 64	920	1.5 TB	QUAD	3	6.0 GB	4.4	16-ICB4 16/32-PSIFB
Z196 2817	1 - 80	1200	3 TB	QUAD w/ shared cache on chip	4	8.0 GB	5.2	32 PSIFB



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Model Configurations

Number of Books	2094 MODELS	Max Engines	2097 MODELS	Max Engines	2817 MODELS	Max Engines
1	S08	8	E12	12	M15	15
2	S18	18	E26	26	M32	32
3	S28	28	E40	40	M49	49
4	S38	38	E56	56	M66	66
4	S54	54	E64	64	M80	80



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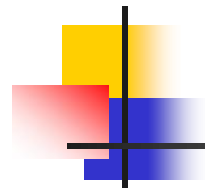
Power

- z10 was introduced as a **green** machine
 - Power requirements increased substantially for the same book configuration when a z10 was compared to a z9.
 - From a MIP perspective the z9 and z10 were neck to neck on a MIPS per WATT comparison
- **z196** uses less power per book (approx .5 KVA) while delivering significantly more MIPS per book.

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z10 User experience

From z9 to z10

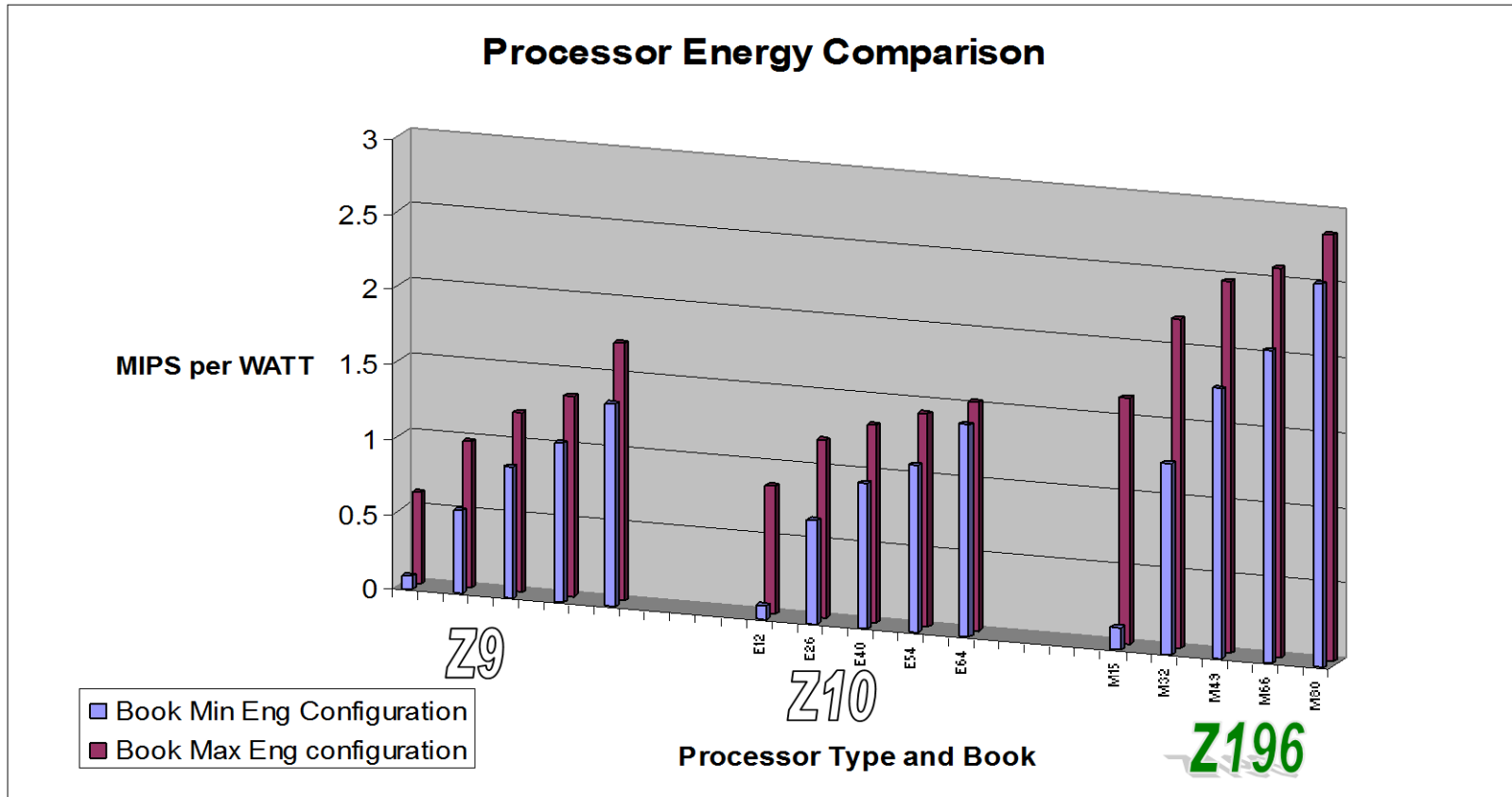


Power Consumption

Book	S54 E56	S38	S54	S54 E56	S54 E56	S18 E26	S38 E56	S18 E26	S28	S38 E56	E40
Model (+ IFA)	724 718	713	725 + 8 IFA	718 713	719 + 8 IFA 715	708 706	715 + 4 IFA 711	708 706	702	709 707	716 + 6 IFA + 4 ICF
KVA	11.717 21.174	11.354	11.509	11.573 20.371	11.716 20.645	9.002 13.659	10.858 20.501	7.053 12.306	8.42	10.23 18.71	15.586
Temp	66.2 66.7	68.2	75.4	72 68.9	73.4 71.6	68.9 66.6	68.5 77.5	69.6 77.2	69.3	69.3 72	72.3

- Temp – Input airflow at 4-5 feet
- Temps over 80+ degrees will cause fans to activate increasing energy required

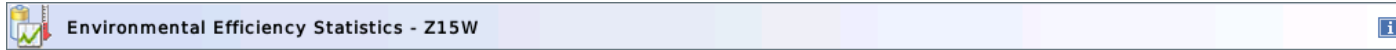

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- These numbers were generated by the power estimation tool.
- Power requirements and MIPS per Book were generated using a minimum and maximum processors per book.

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HMC Environmental Display

 Environmental Efficiency Statistics - Z15W 

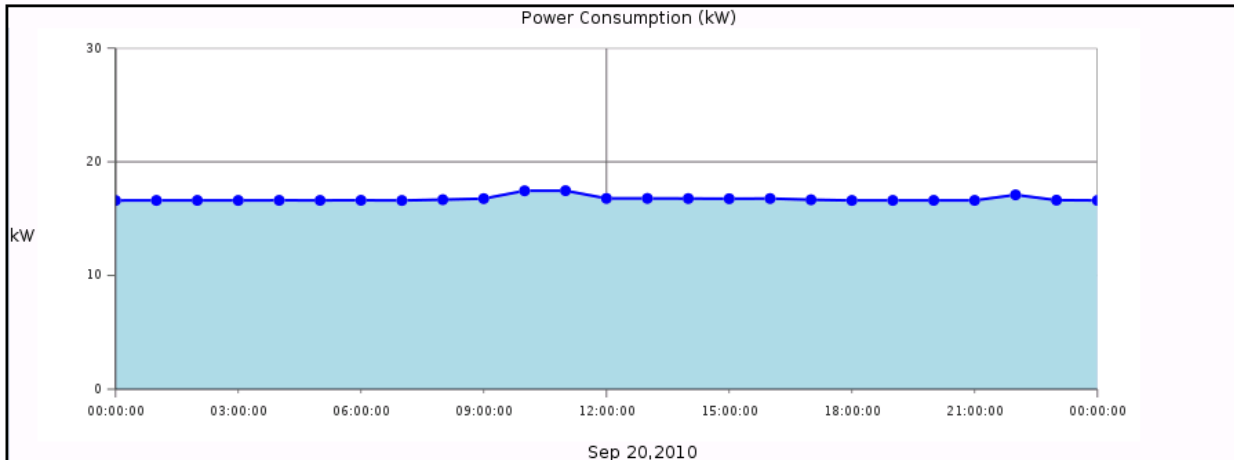
To display new data, enter the start date and/or the duration, and click Refresh.

Starting date: Duration:



Date and Time	Power Consumption (kW)	Power Consumption (Btu/hr)	Temperature (°C)	Temperature (°F)	CP Utilization (%)
Sep 20, 2010 12:00:00 AM	16.596	56628	23.5	74.3	11
Sep 20, 2010 1:00:00 AM	16.601	56645	23.5	74.3	11
Sep 20, 2010 2:00:00 AM	16.603	56652	23.5	74.3	11
Sep 20, 2010 3:00:00 AM	16.599	56638	23.5	74.3	11
Sep 20, 2010 4:00:00 AM	16.607	56665	23.5	74.3	11
Sep 20, 2010 5:00:00 AM	16.603	56652	23.5	74.3	11
Total: 25					

Chart Content:



- **Graphic display over time**
- **Screen capture support** valuable for providing operations documentation

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Enhanced Activity Display

Monitors Dashboard

Pause Display Open Activity Open Activity Profiles

Overview

--- Select Action --- Filter

Select	System	Processor Usage (%)	Channel Usage (%)	Power Consumption (kW) (Btu/hr)	Input Air Temperature (°C) (°F)
<input type="checkbox"/>	Z15W		47	22 16.594 56,621.078	

Page 1 of 1 Max Page Size: 100 Total: 1 Filtered: 1 Displayed: 1 Selected: 0

Details

Z15W

Power Consumption

Name	Power Consumption (kW) (Btu/hr)
None	
Total: 0	

Aggregated Processors

Type	All Processor Usage (%)	Shared Processor Usage (%)
GP		12
ICF		63
IFL		0
IIP		2
CP		20
Total: 5		

System Assist Processors

Name	Processor Usage (%)
SAP00	
SAP01	
SAP02	
SAP03	
SAP04	

Input Air Temperature

Name	Input Air Temperature (°C) (°F)
None	
Total: 0	

Processors

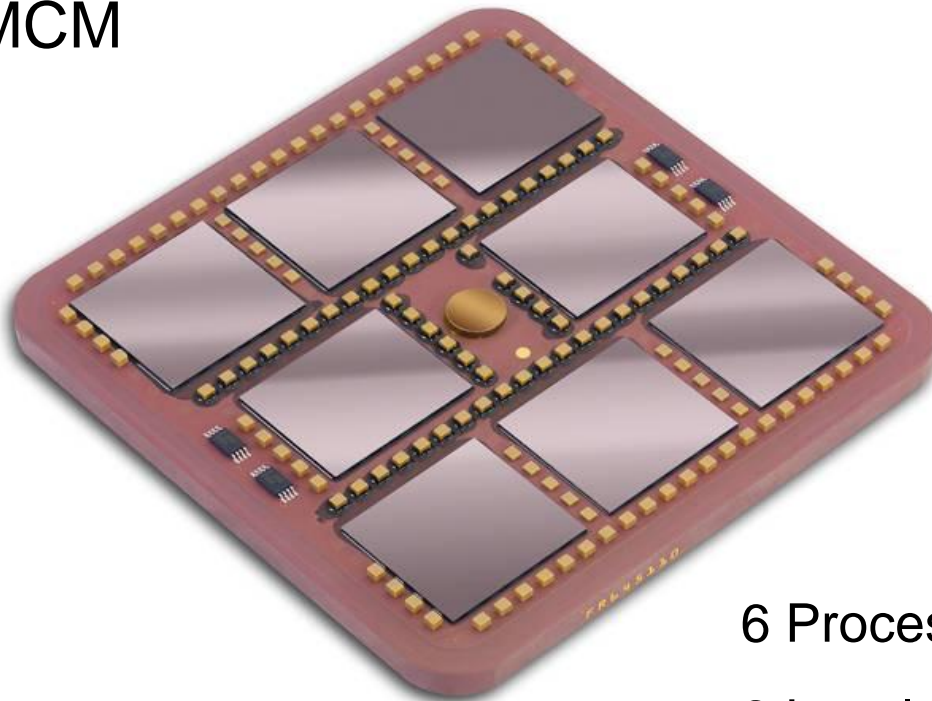
Name	Processor Usage (%)
GP00	
GP01	
GP02	
GP03	
GP04	
Total: 47	

Logical Partitions

Name	Processor Usage (%)
AEVM	
AEV2	
AE91	
AE92	
CFC	

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MCM



6 Processor Chips

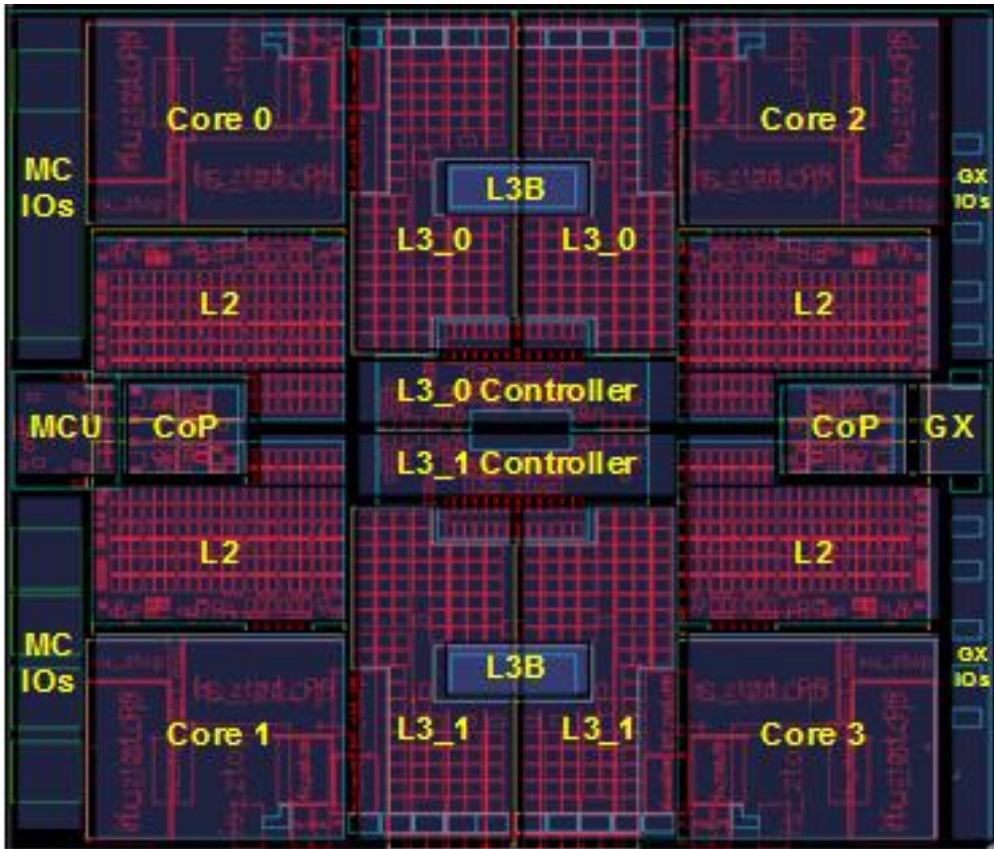
2 Level 4 cache Chips

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2817 Model Characteristics by Book

Model	1 st Book			2nd Book			3rd Book			4th Book			Max Memory for Model
	Avail CPs	SAPs	Spares	Avail CPs	SAPs	Spares	Avail CPs	SAPs	Spares	Avail CPs	SAPs	Spares	
M15	15	3	2										752 GB
M32	16	3	1	16	3	1							1520 GB
M49	16	3	1	16	3	1	17	3	0				2288G B
M66	16	3	1	16	3	1	17	3	0	17	3	0	3056G B
M80	20	3	1	20	3	1	20	4	0	20	4	0	3056G B

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Processor Chip

- 4 Cores 3 cache levels
- Level 1 cache - 128/64 KB
- Level 2 cache - 1.5 MB
formally known as level 1.5 cache
- Level 3 cache - 24 MB shared by all cores on a chip

Level 4 cache is on 2 separate
96 MB Chips for 192 MB total



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Cache Comparison

z10	Cache Level 1	Cache Level 1.5	Cache Level 2	
	128k Data 64k Instr	3 MB	book cache	
z196	Cache Level 1	Cache Level 2	Cache Level 3	Cache Level 4
	128k Data 64k Instr	1.5 MB	Cores on chip share	book cache



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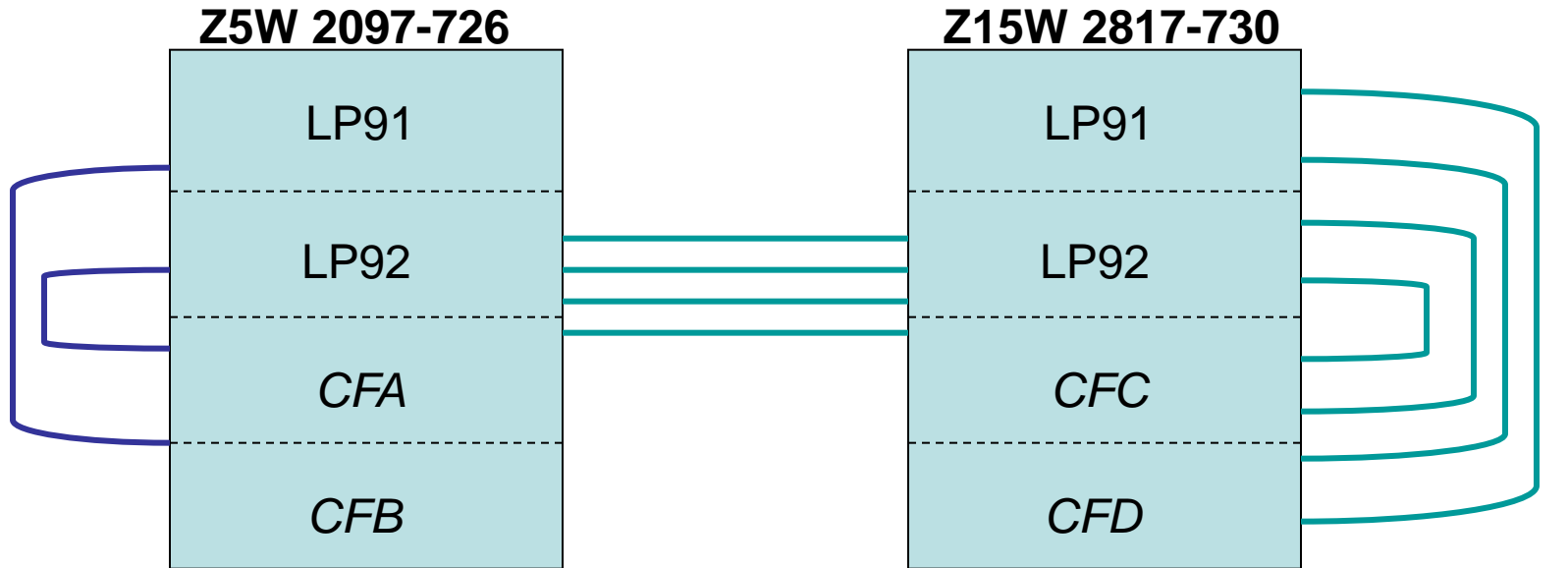
Hiperdispatch

Hiperdispatch characteristics are an evolving science

- The Hypervisor continues to align physical processors vertically to a subset of logical processors (as introduced with the z10)
- WLM's management of the Affinity nodes has evolved.
 - Node affinity scope has changed from same book to same core (sharing level 3 cache influences this change)
 - WLM now places work on a weighted basis on the affinity nodes. 4 core chips/nodes are assigned more work than a 3 core chip.

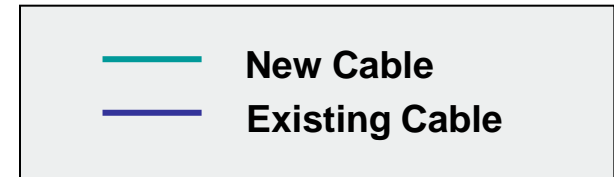
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ESP Testing Configuration



Notes:

- z/OS LPARs may exist on either machine
- CF LPARs
- Z5W has 6 ICF engines
- Z15W has 8 ICF engines



PSIFB LINKS

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RMFIII

```
Samples: 60      System: AE92  Date: 06/30/10  Time: 18.01.00  Range: 60
Partition:      AE92      2817 Model 734
CPC Capacity:   3013      Weight % of Max: ****  4h Avg:      5      Group:      N/A
Image Capacity: 1595      WLM Capping %:      0.0  4h Max:     223     Limit:      N/A

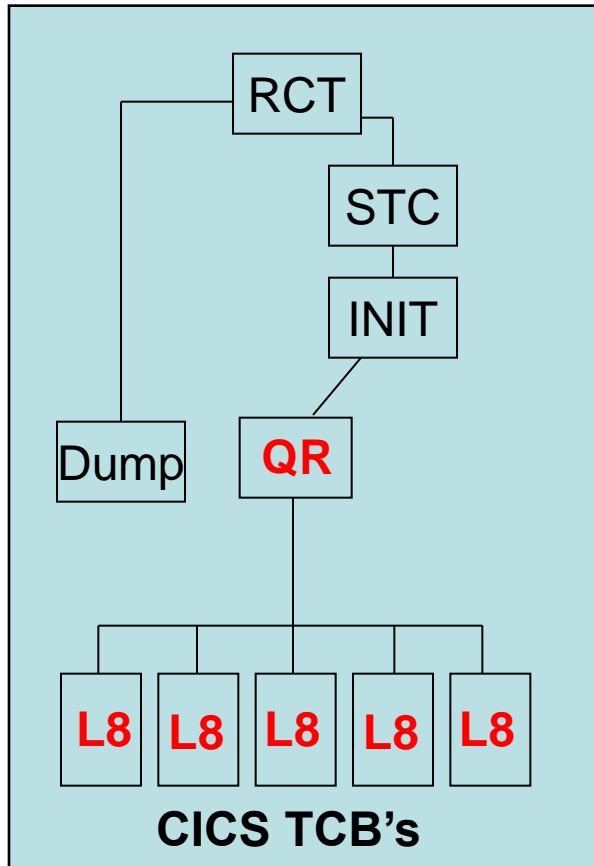
Partition  --- MSU  ---  Cap  Proc  Logical  Util %  - Physical Util % -
           Def  Act  Def  Num  Effect  Total  LPAR  Effect  Total
*CP                               12.0      0.1      7.5      7.6
AE92              0  227  NO  12.0      21.2     21.4     0.1      7.5      7.5
PHYSICAL                               0.1                               0.1
```

Omegamon

```
LPAR
+ Model = 2817-734  Serial = 0D7425      CEC MSUs capacity = 3134
+ Number of Physical processors = 47      Dispatch interval = DYNAMIC
+ Number of CPs = 34  Special CPs = 13    Elapsed interval = 00.00.01.005
+
```

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Testing Background



CICS TCB Structure

QR (Quasi Re-entrant) TCB (aka **APP**)

- All application Cobol work
- Many transactions serially serviced
- Dispatch managed by CICS

L8 TCB's

- DB2 and MQ applications execute on L8's
- Parallel execution
- Dispatch managed by MVS operating system

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CICS TRANSACTION KEY

Tran Name	Threadsafe	Description
GHDL	No	MQ 100 - .25 MS WAITS + 16 Million instructions per POST
GHC1	YES	1100 fetches per tran out of cache
GHC2	NO	1100 fetches per tran out of cache
GHI0	NO	1000-1100 fetches per tran prefetch I/O
GHI1	YES	1000-1100 fetches per tran prefetch I/O

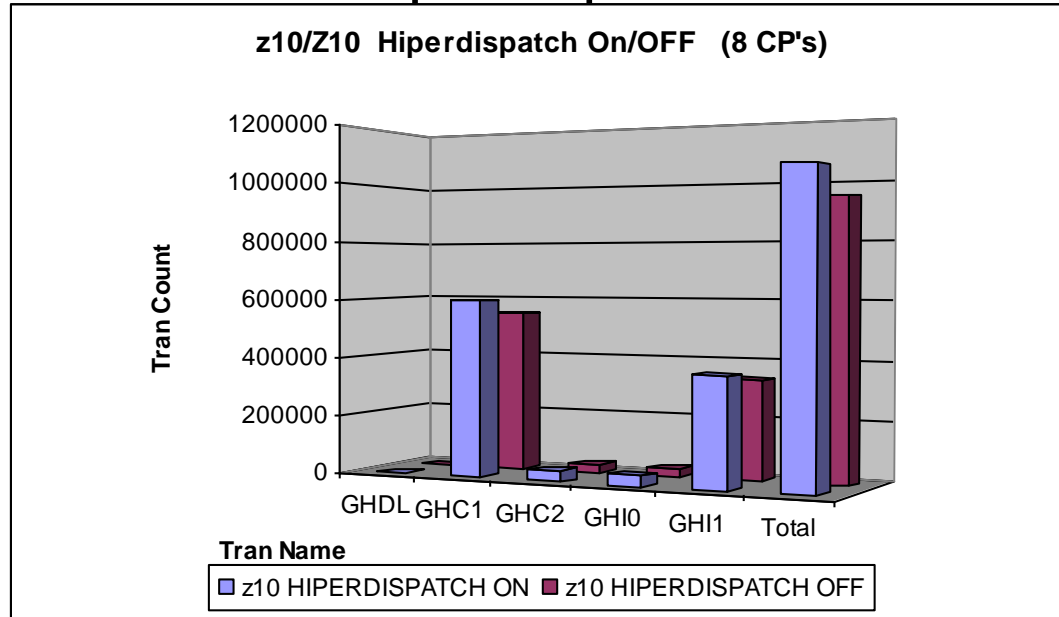
Transaction Driver - completion based initiation

Reads MQ Queue for transaction specifications for:

- Duration
- Transaction name
- Transaction concurrency

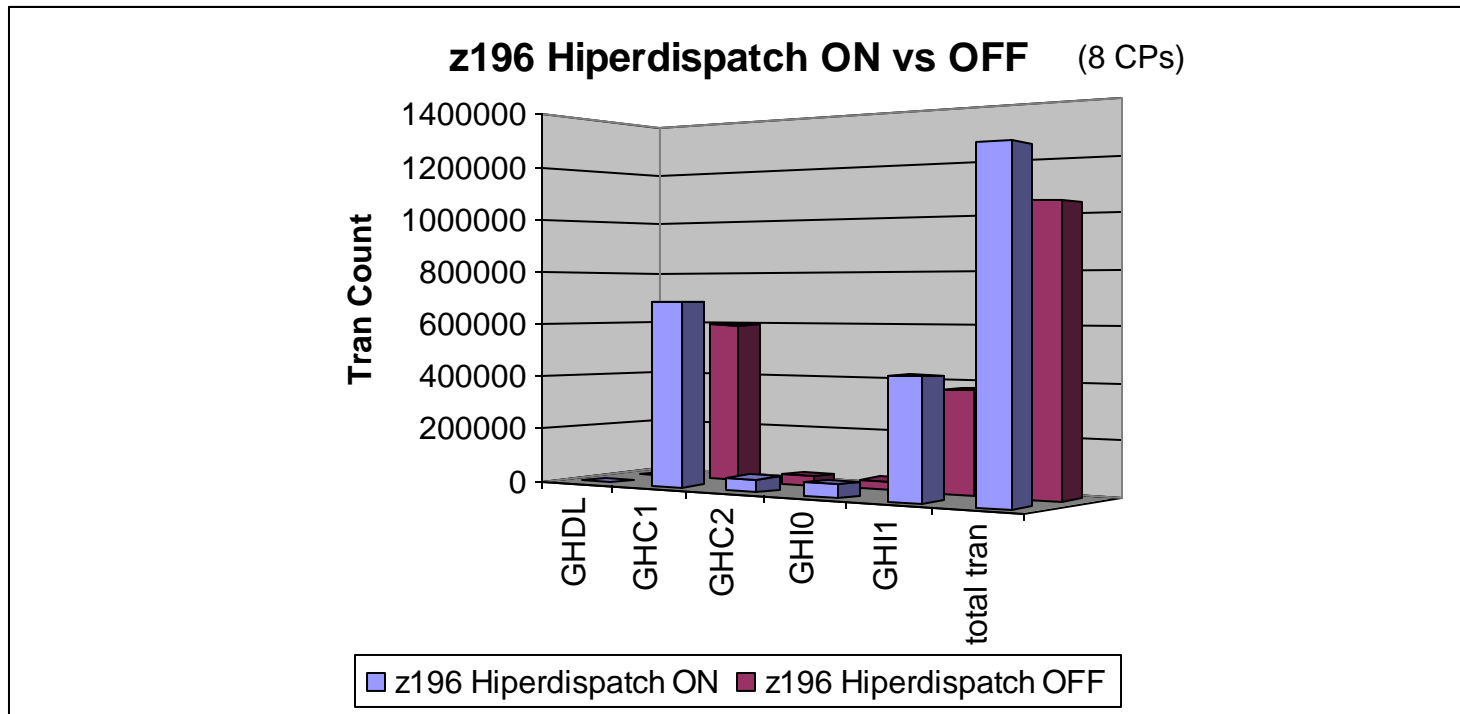
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Hiperdispatch



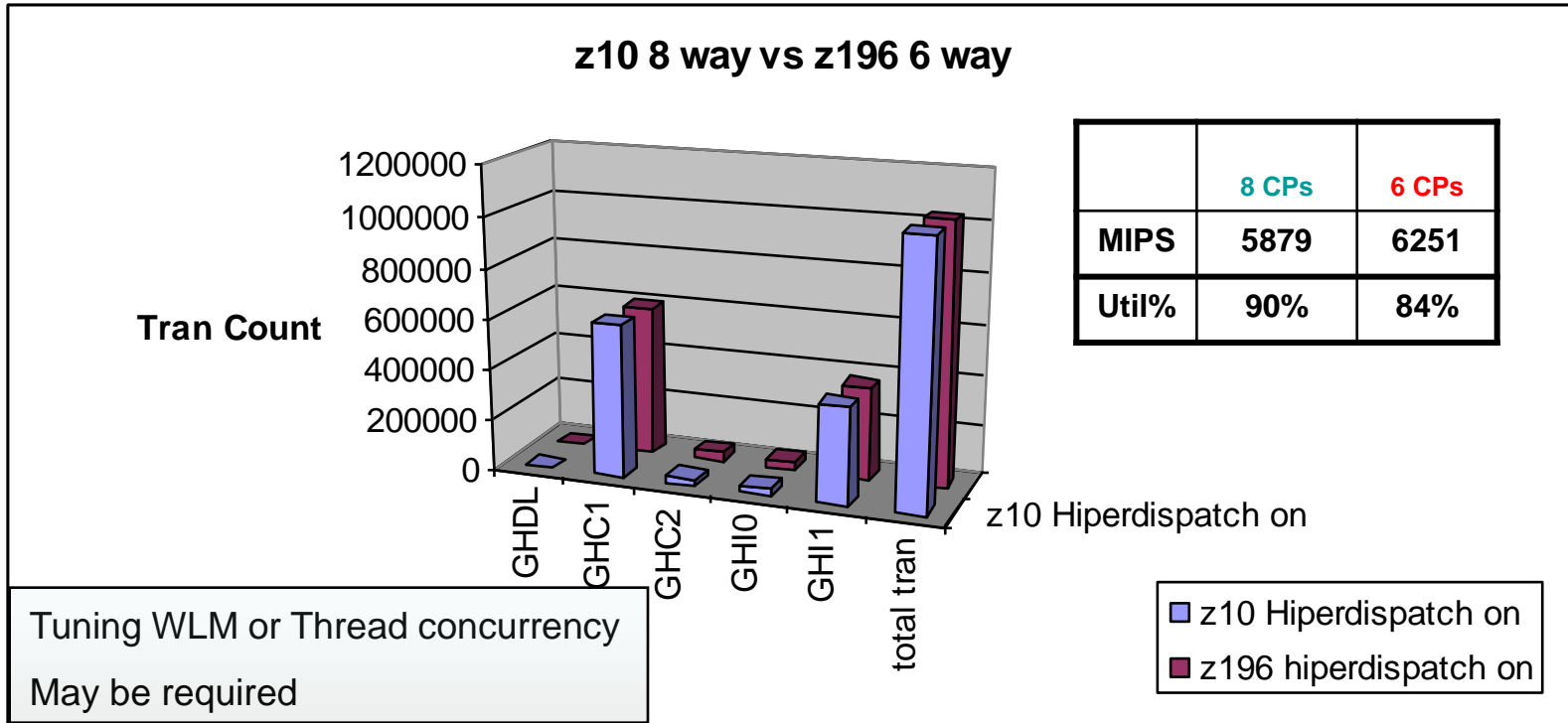
Tran	GHDL	GHC1	GHC2	GHI0	GHI1	total tran
z10 Hiperdispatch ON	160	598667	36133	35100	367649	1037709
z10 Hiperdispatch OFF	144	551831	27873	27667	338888	946403
Tran delta	16	46836	8260	7433	28761	91306
% delta	11.11%	8.49%	29.63%	26.87%	8.49%	9.65%

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Tran	GHDL	GHC1	GHC2	GHI0	GHI1	total tran
z196 Hiperdispatch ON	180	688194	48813	47881	433296	1218364
z196 Hiperdispatch OFF	168	596079	34169	34001	373456	1037873
Tran delta	12	92115	14644	13880	59840	180491
% delta	7.14%	15.45%	42.86%	40.82%	16.02%	17.39%

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	GHDL	GHC1	GHC2	GHI0	GHI1	total tran
z196 Hiperdispatch ON	172	604553	26864	26853	383130	1041572
z10 Hiperdispatch ON	160	598667	36133	35100	367649	1037709
Tran delta	12	5886	-9269	-8247	15481	3863
% delta	7.50%	0.98%	-25.65%	-23.50%	4.21%	0.37%



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Hiperdispatch

- The z196 processor rewards your ability to hold a dispatch!
- MIPS are nice but point of dispatch must also be considered
- Chatty workloads (CICS QR for example) vs Batch or CICS Threadsafe lose ground to workloads that hold that their dispatch.
- When the point of dispatch is reduced and the MIPS per engine is increased the capability of the QR throughput increases from an engine perspective. BUT the competition for that engine also increases
- Machine upgrades often result in more MIPS being delivered by a reduced number of engines.
- Tuning WLM goals or managing concurrency may be required!

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SYSID	Mon	Day	SH	Hour	CPI	Prb State	Est Instr Cmplx CPI	Est Finite CPI	Est SCPL1M	L1MP	L2P	L3P	L4LP	L4RP	MEMP	Rel Nest Intensity	LPARCPU	Eff GHz	CICS
PAR1	SEP	1	P	16	7.0	31.8	2.8	4.2	50	8.5	69.3	19.0	7.6	3.4	0.7	0.46	1459.4	5.2	QR
PAR2	SEP	1	P	16	4.7	23.4	3.0	1.7	24	7.0	89.2	5.6	4.5	0.1	0.7	0.20	1546.2	5.2	Threadsafe

- Benchmark Description
 - Comprises of CICS transactions and some Batch...
 - All Batch is heavy Update and running on both LPARs
 - The CICS transactions are cloned pairs. One group is left to run in QR mode and the other is marked threadsafe in the CICS PPT definition. This test Focused all the Quasi-Reentrant transactions in one LPAR and all the Threadsafe transactions in the other LPAR. Transaction concurrency was establish in order to drive the LPARs to 90%+ utilization levels.
- Threadsafe Vs QR Results
 - CICS 110s
 - Increase of 52% of transactions
 - Decrease of 42% in CPU per Transaction
 - Decrease of average response time by 67% (3.0x)
 - RMF 72s – CICS Storage Class
 - Ended Transactions up 2.4x
 - Response Time down 3.6x
 - SMF 113s – LPAR
 - CPI down 1.48x from 7.0 to 4.7
 - L1MP down 1.5% from 8.5% to 7.0%
 - L2P up 19.9% from 69.3% to 89.2%

CICS Threadsafe is an option that may help you reduce CPU cost for applicable transactions by reducing switches between different TCB types

CPU MF example to supplement CICS and RMF performance metrics

As a secondary data source to understand why performance may have changed

These numbers come from a synthetic Benchmark and do not represent a production workload



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HIS comparison of a LPAR running Threadsafe vs a QR LPAR workload

SYSID	Mon	Day	SH	Hour	CPI	Prb State	Est Instr Cmplx CPI	Est Finite CPI	Est SCPL 1M	L1MP
AE91	SEP	1 P		16.00	7.0	31.8	2.8	4.2	50	8.5
AE92	SEP	1 P		16.00	4.7	23.4	3.0	1.7	24	7.0

L2P	L3P	L4LP	L4RP	MEMP	Rel Nest Intensity	LPARCPU	Eff GHz	CICS	CICSTRX2 Ended Transactions	CICSTRX2 Response Time
69.3	19.0	7.6	3.4	0.7	0.46	1459.4	52	QR	1,874,005	0.11
89.2	5.6	4.5	0.1	0.7	0.20	1546.2	52	Threadsafe	4,555,108	0.03

Same run as previous foil but includes CICS trans data

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SYSID	Mon	Day	SH	Hour	CPI	Prb State	Est Instr Cmplx CPI	Est Finite CPI	Est SCPL1M	L1MP	L15P	L2LP	L2RP	MEMP	Rel Nest Intensity	LPARCPU	Eff GHz	Ded/Shr
AE83	JUN	1	P	TOTAL	6.87	15.4	3.0	3.9	88	4.4	69.5	23.9	0.1	6.6	0.73	464.7	4.40	Ded
AE83	JUN	2	P	TOTAL	7.27	14.9	3.2	4.1	93	4.4	67.2	25.8	0.1	6.9	0.78	612.8	4.40	Ded
AE83	JUN	3	P	TOTAL	6.43	12.5	2.9	3.6	93	3.8	67.3	25.5	0.1	7.1	0.79	627.6	4.40	Ded
AE83	JUN	4	P	TOTAL	7.14	14.8	3.2	4.0	91	4.4	67.5	25.6	0.1	6.8	0.77	553.4	4.40	Ded
	Average				6.93	14.4	3.1	3.9	91	4.3	67.9	25.2	0.1	6.9	0.77	564.6		Ded
AE83	MAY	25	P	TOTAL	7.66	17.6	3.2	4.5	87	5.2	68.6	25.4	0.1	6.0	0.70	641.6	4.40	Shr
AE83	MAY	26	P	TOTAL	7.36	16.1	3.1	4.3	87	4.9	69.0	24.7	0.1	6.3	0.72	621.1	4.40	Shr
AE83	MAY	27	P	TOTAL	7.31	14.5	3.1	4.2	88	4.8	68.5	25.0	0.1	6.4	0.73	395.6	4.40	Shr
	Average				7.44	16.0	3.1	4.3	87	5.0	68.7	25.0	0.1	6.2	0.72	552.8		Shr
Dedicated / Shared					0.93	0.90	0.98	0.90	1.04	0.86	0.99	1.01	0.98	1.11	1.07	1.02		
					1.07	Relative ITR Capacity Ratio Of Dedicated Vs Shared												

CPI – Cycles per Instruction

Prb State - % Problem State

Est Instr Cmplx CPI – Estimated Instruction Complexity CPI (infinite L1)

Est Finite CPI – Estimated CPI from Finite cache/memory

Est SCPL1M – Estimated Sourcing Cycles per Level 1 Miss

L1MP – Level 1 Miss %

L15P – % sourced from Level 2 cache

L2LP – % sourced from Level 2 Local cache (on same book)

L2RP – % sourced from Level 2 Remote cache (on different book)

MEMP - % sourced from Memory

Rel Nest Intensity – Reflects distribution and latency of sourcing from shared caches and memory

LPARCPU - APPL% (GCPs, zAAPs, zIIPs) captured and uncaptured

Eff GHz – Effective gigahertz for GCPs, cycles per nanosecond



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DB2 V10 testing - HIS data

Field defs on next page

	CPI	PRBSTATE	L1MP	L2P	L3P	L4LP	L4RP	LPARBUS	MEMP	MIPSEXE	ESTICCPI	ESTFINCF	ESTSCP1	IRNI	EFFGHZ	TLB1MISS	TLB1CYCL	PTEPCTM	SYSTEM
05JAN2011:06:59:	5.3	25.7	8.5	85.1	8.3	4.3	1.5	1633.5	3.9	15971.4	2.7	2.6	31.3	0.7	5.2	8.5	41.4	15.9	AE91
05JAN2011:07:59:	5.4	25.6	8.4	85.0	8.4	4.3	1.5	1654.7	3.9	16092.4	2.7	2.6	31.3	0.6	5.2	8.5	41.8	16.0	AE91
05JAN2011:06:59	5.1	25.6	8.4	85.2	8.2	5.0	0.8	1614.3	4.5	16506.5	2.6	2.5	29.7	0.7	5.2	8.6	42.0	16.9	AE92
05JAN2011:07:59	5.1	25.3	8.4	85.0	8.3	5.0	0.8	1636.0	4.5	16637.0	2.6	2.5	29.9	0.7	5.2	8.7	42.4	17.2	AE92
06JAN2011:06:59	5.3	25.6	8.4	84.9	8.4	4.3	1.5	1637.1	3.9	16006.6	2.7	2.6	31.1	0.6	5.2	8.5	42.9	18.0	AE91
06JAN2011:07:59	5.3	26.4	8.3	84.9	8.4	4.3	1.5	1664.2	3.9	16479.4	2.7	2.6	31.1	0.6	5.2	8.5	43.2	18.1	AE91
06JAN2011:06:59	5.1	25.3	8.4	85.0	8.3	5.0	0.8	1622.1	4.5	16543.5	2.6	2.5	29.8	0.7	5.2	9.1	44.1	18.8	AE92
06JAN2011:07:59	5.1	25.1	8.3	85.1	8.3	5.0	0.8	1641.7	4.5	16836.4	2.6	2.5	29.8	0.7	5.2	9.1	44.2	18.9	AE92

- AE91 had 7.5GB (20%) large page allocated
- AE92 had **NO** Large Page allocated
- BP's were Pagefix=yes on Jan05 and Pagefix=no on Jan 6



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HIS Field Definitions

CPI	NUM	8	6.1	CYCLES*PER*INSTRUCTION
EFFGHZ	NUM	8	6.1	EFFECTIVE*GIGAHERTZ*CYCLES*PER NAND
ESTFINCP	NUM	8	6.1	ESTIMATED*CPI FROM*FINITE*CACHE/MEM
ESTICCP	NUM	8	6.1	ESTIMATED*INSTRUCTION*COMPLEXITY*CPI
ESTSCP1M	NUM	8	6.1	ESTIMATED*SOURCING*CYCLES*PER L1 MISS
LPARBUSY	NUM	8	6.1	LPARCPU*PERCENT*CAPTURED AND*UNCAPTURED
L1MP	NUM	8	6.1	LEVEL*1*MISS*PERCENT
L15P	NUM	8	6.1	PERCENT*SOURCED*FROM*L1.5*CACHE
L2LP	NUM	8	6.1	PERCENT*SOURCED*FROM*L2*SAME BOOK
L2P	NUM	8	6.1	PERCENT*SOURCED*FROM*L2*CACHE
L2RP	NUM	8	6.1	PERCENT*SOURCED*FROM*L2*DIFFERENT*BOOK
L3P	NUM	8	6.1	PERCENT*SOURCED*FROM*L3*SAME CHIP CACHE
L4LP	NUM	8	6.1	PERCENT*SOURCED*FROM*L4*SAME BOOK
L4RP	NUM	8	6.1	PERCENT*SOURCED*FROM*L4*DIFFERENT*BOOK
MEMP	NUM	8	6.1	PERCENT*SOURCED*FROM*MEMORY
MIPSEXC	NUM	8		EXECUTED*MIPS
PRBSTATE	NUM	8	6.1	PERCENT*PROBLEM*STATE
PTEPCTMI	NUM	8	6.1	PAGETABLE*ENTRY*PCT OF TLB*MISSSES
RNI	NUM	8	6.1	RELATIVE*NEST*INTENSITY
TLB1CYCL	NUM	8	6.1	CYCLES*PER*TLB*MISS
TLB1MISS	NUM	8	6.1	TLB*CPU MISS*PERCENT OF*TOTAL CPU



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DB2 V10 testing - HIS Observations

Comparing AE91 to AE92

- TLB1MISS improved 1.8% with Large Page
- TLB1CYCL Improved 1.9% with Large Page
- PTEPCTMI showed a 6.9% improvement with Large Page

-
- CPI increased 4.7% with Large Page
 - PRBSTATE showed an improvement of 3.5% with Large Page
 - ESTICCPI increased 3.7%
 - MIPSEEXEC showed an improvement of 3.4% with Large Page



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DB2 V10 testing - HIS Conclusions

Large Page processing by DB2 showed an increase in the CPI (Cycles Per Instruction) which must be weighed by the fact that the PRBSTATE mix of instructions increased. The instruction complexity increased 3.7% and indicated by the ESTICCPI.

This indicates that the productive processing or application machine path (business logic vs service support) consumed a greater portion of our processor capacity.

Overall we seem to have gained about 2% in productivity which becomes meaningful in an installation with 124 CPs and 21 zAAP engines.

Another factor to consider is the fact that the AE91 LPAR sourced a L4 cache from the local book 16% less than AE92 (L4LP) and increase the access to L4RP (remote book) by 46%.

Based on these findings Large Page will be implemented at Aetna for DB2 V10.

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zIIP consumption in DB2 V10 was a pleasant finding as they were not observed in DB2 V9. The DBM1 address space shows zIIP consumption attributed to an Enclave that appears to be classified under the MSTR address space.

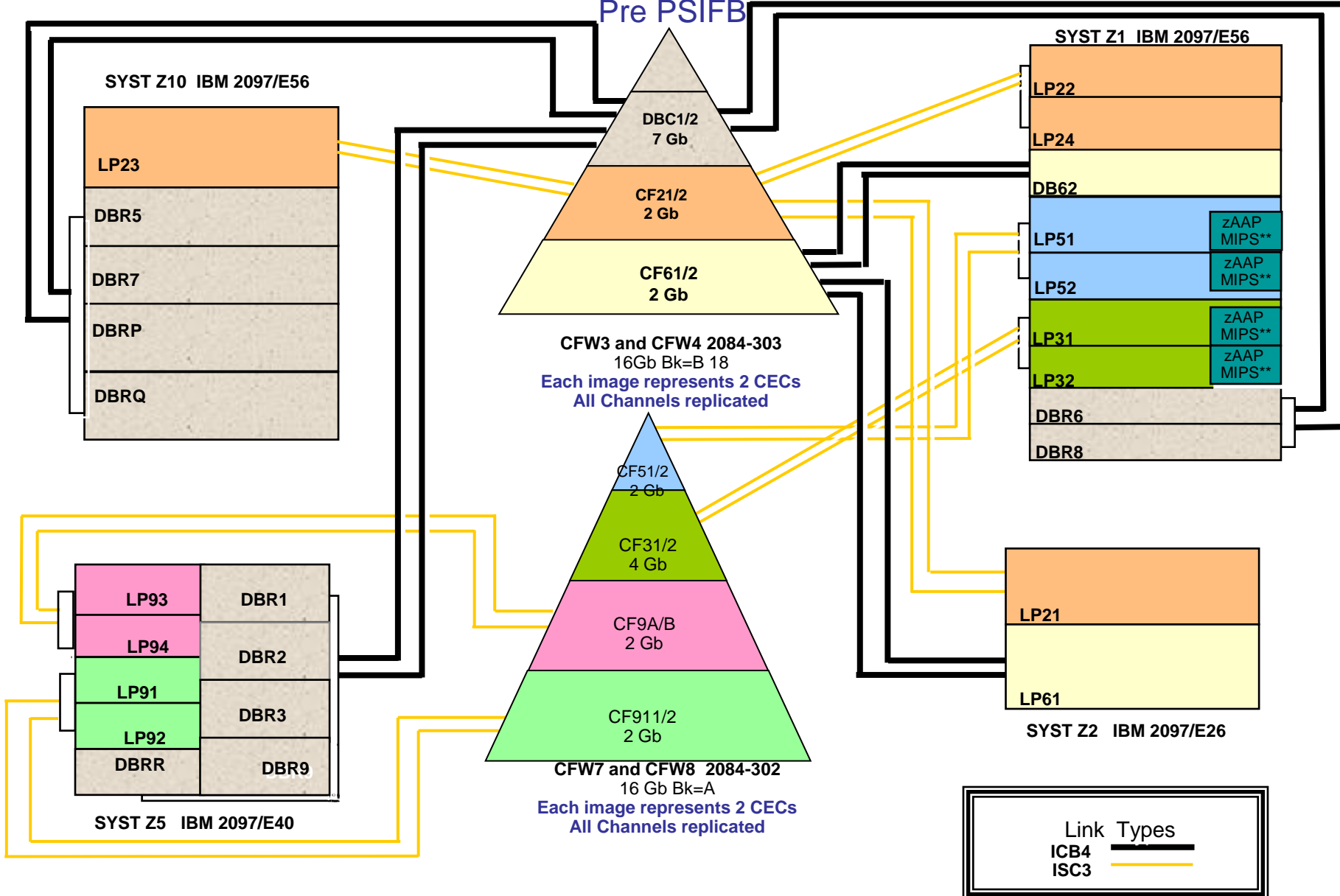
Samples: 1799 System: AE92 Date: 01/05/11 Time: 08.03.00 Range: 1800 Sec

Service			--- Time on CP % ---			----- EApp1 % -----		
Jobname	CX	Class	Total	AAP	IIP	CP	AAP	IIP
T8D1EASM	B0	ONLIS01	230.7	0.0	0.0	230.7	0.0	0.0
T8D1EASP	B0	ONLIS01	229.8	0.0	0.0	229.8	0.0	0.0
T8D1EAS0	B0	ONLIS01	228.7	0.0	0.0	228.7	0.0	0.0
T8D1EASN	B0	ONLIS01	228.4	0.0	0.0	228.4	0.0	0.0
T8D1EASQ	B0	ONLIS01	227.7	0.0	0.0	227.7	0.0	0.0
T8D1EASR	B0	ONLIS01	227.6	0.0	0.0	227.6	0.0	0.0
DBPBDBM1	S	SYSSTC	18.2	0.0	0.0	18.3	0.0	25.9
DBUBP921	B	BATIS003	8.9	0.0	0.0	8.9	0.0	0.0
DBUBP925	B	BATIS003	8.9	0.0	0.0	8.9	0.0	0.0

Windsor Computer Center

CPU Configuration

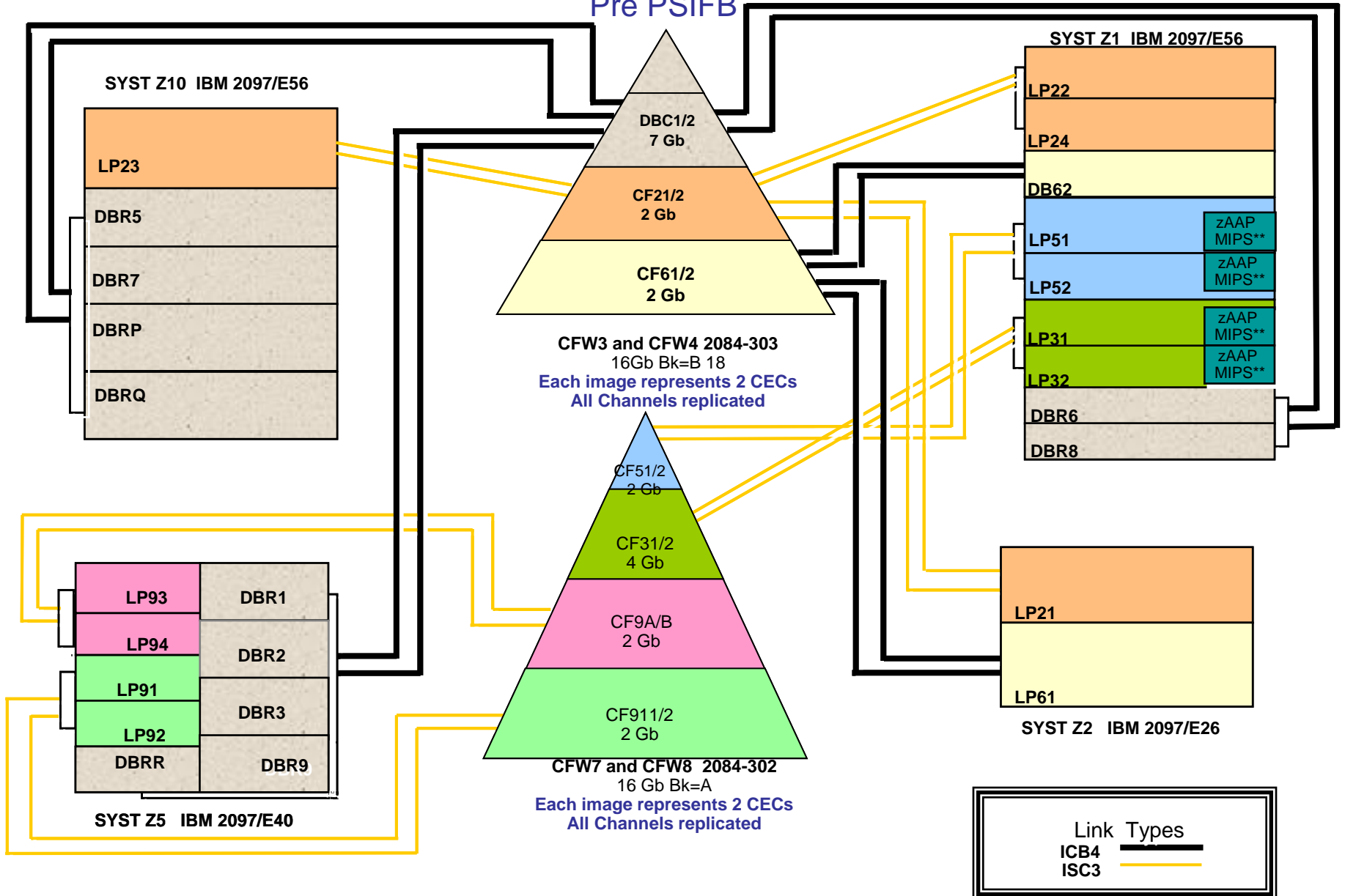
Pre PSIFB



Windsor Computer Center

CPU Configuration

Pre PSIFB

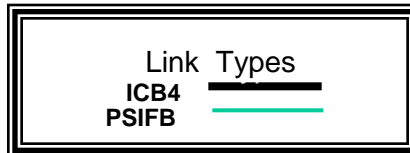
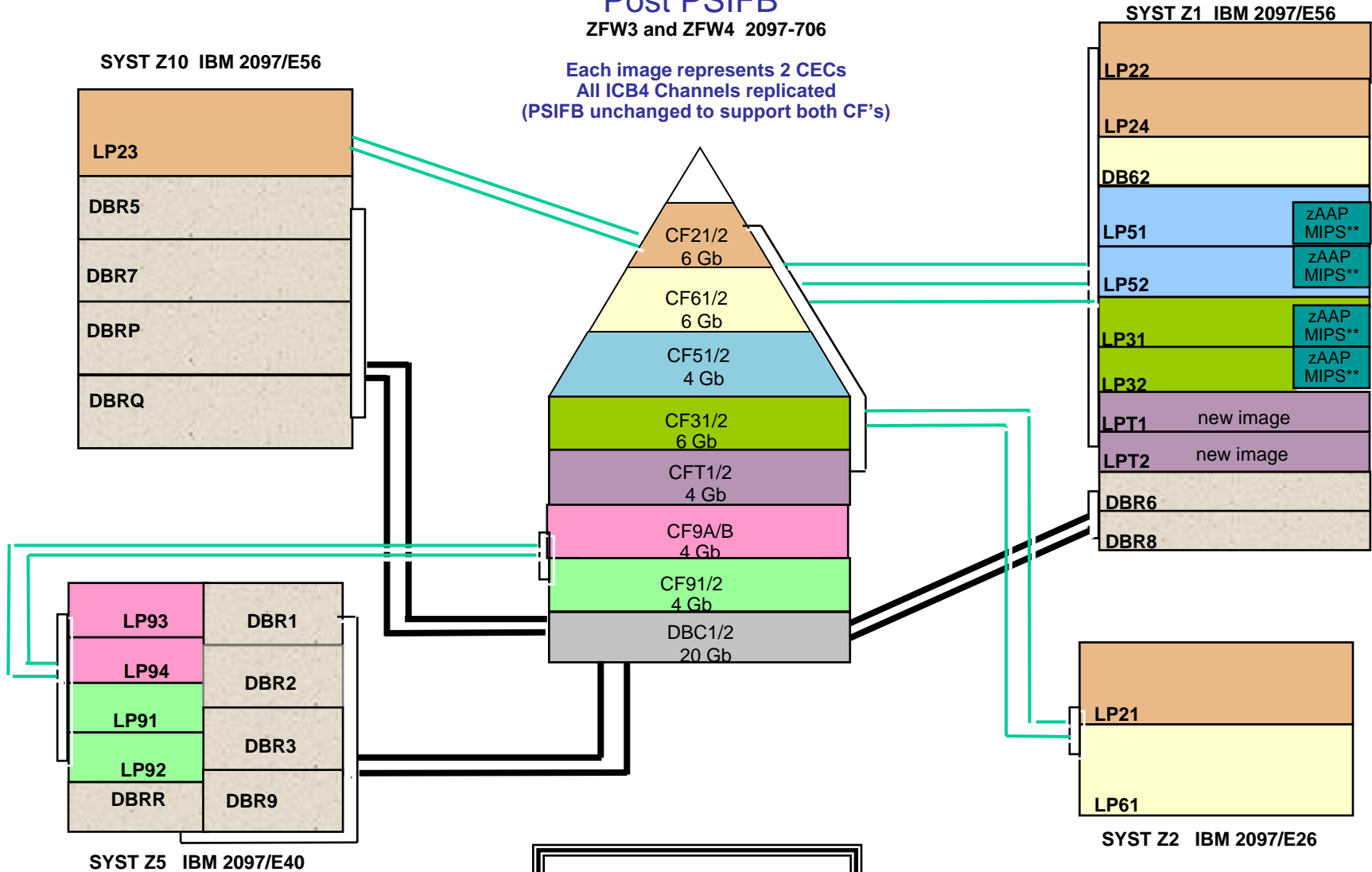


Windsor Computer Center

CPU Configuration Post PSIFB

ZFW3 and ZFW4 2097-706

Each image represents 2 CECs
All ICB4 Channels replicated
(PSIFB unchanged to support both CF's)

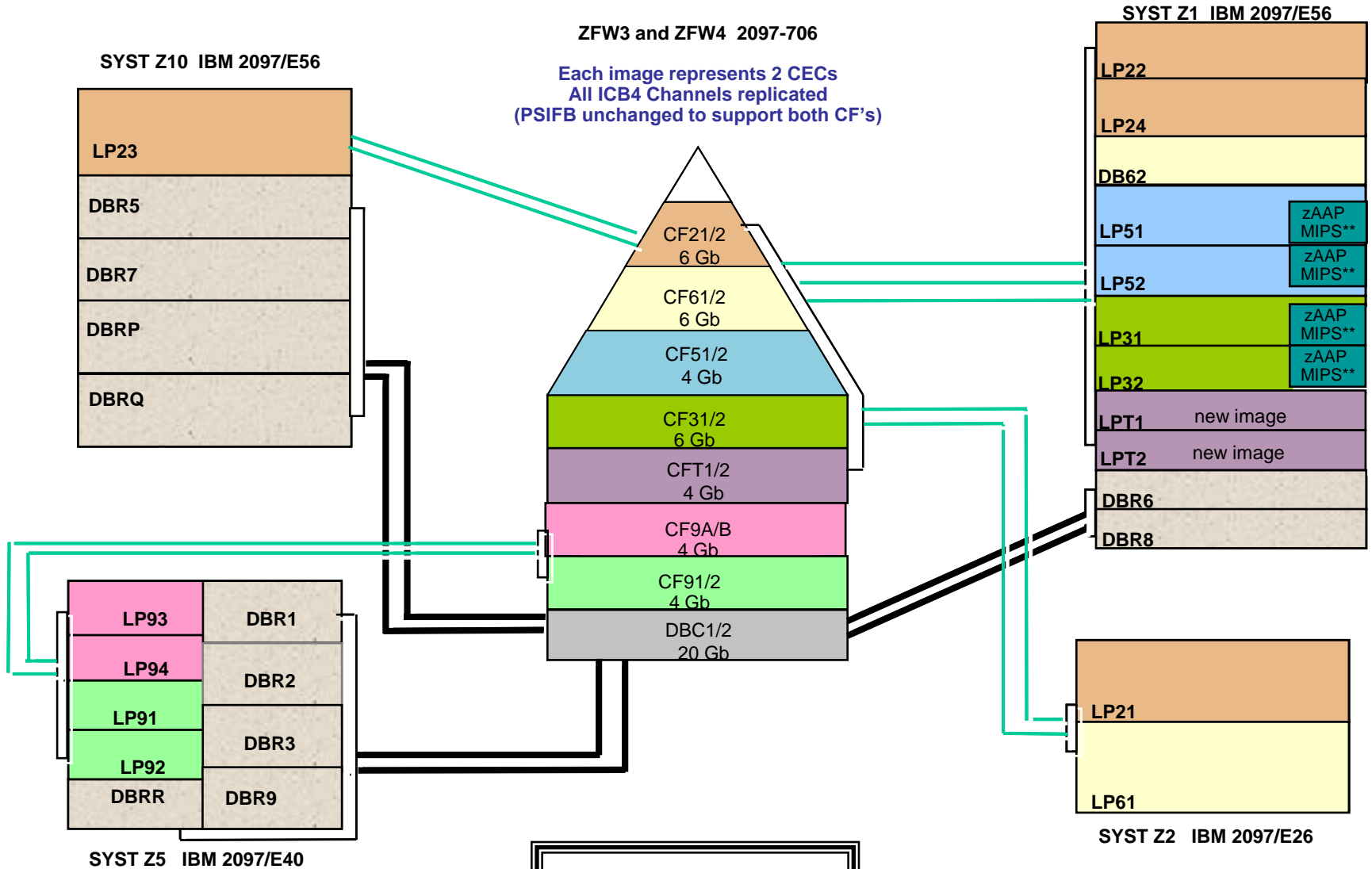


Windsor Computer Center

CPU Configuration Post PSIFB

ZFW3 and ZFW4 2097-706

Each image represents 2 CECs
All ICB4 Channels replicated
(PSIFB unchanged to support both CF's)

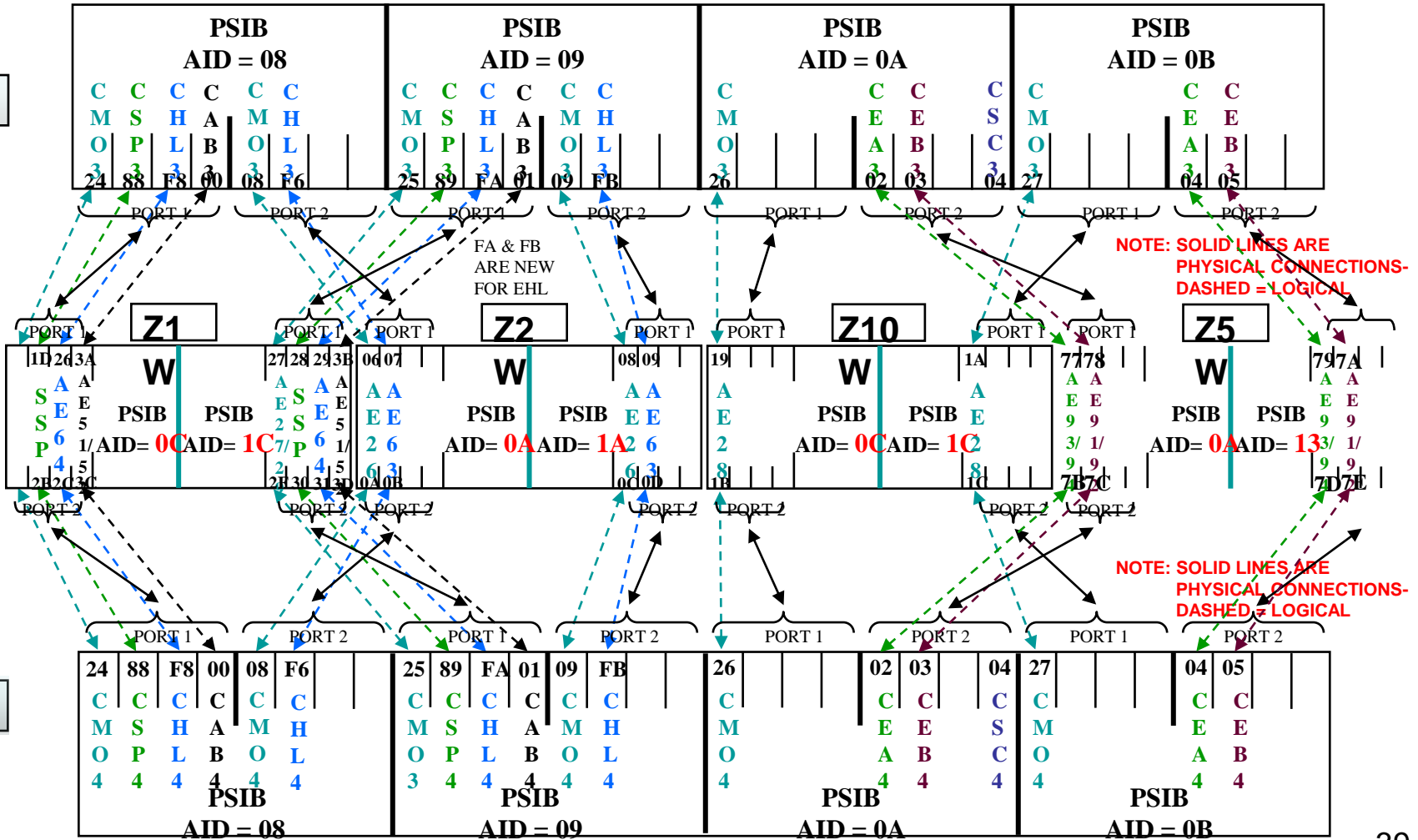


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PSIFB Connectivity

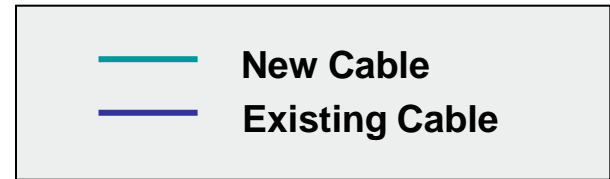
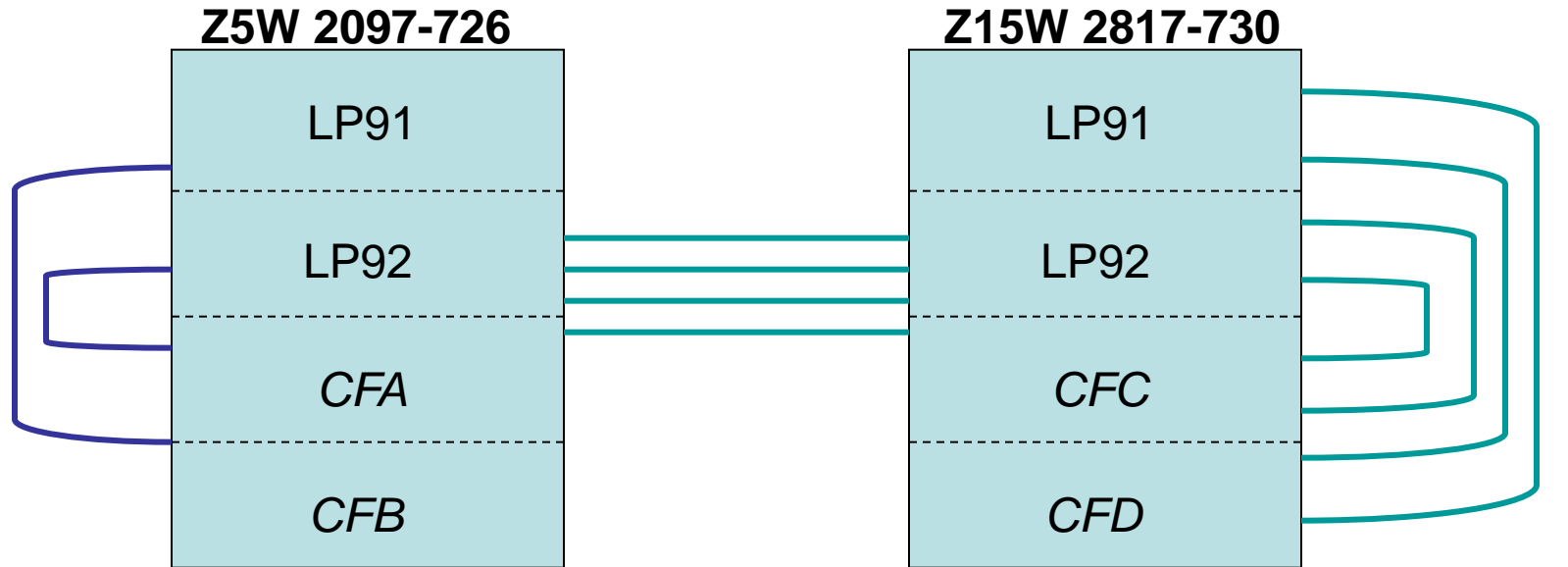
CF1

CF2



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ESP Testing Configuration

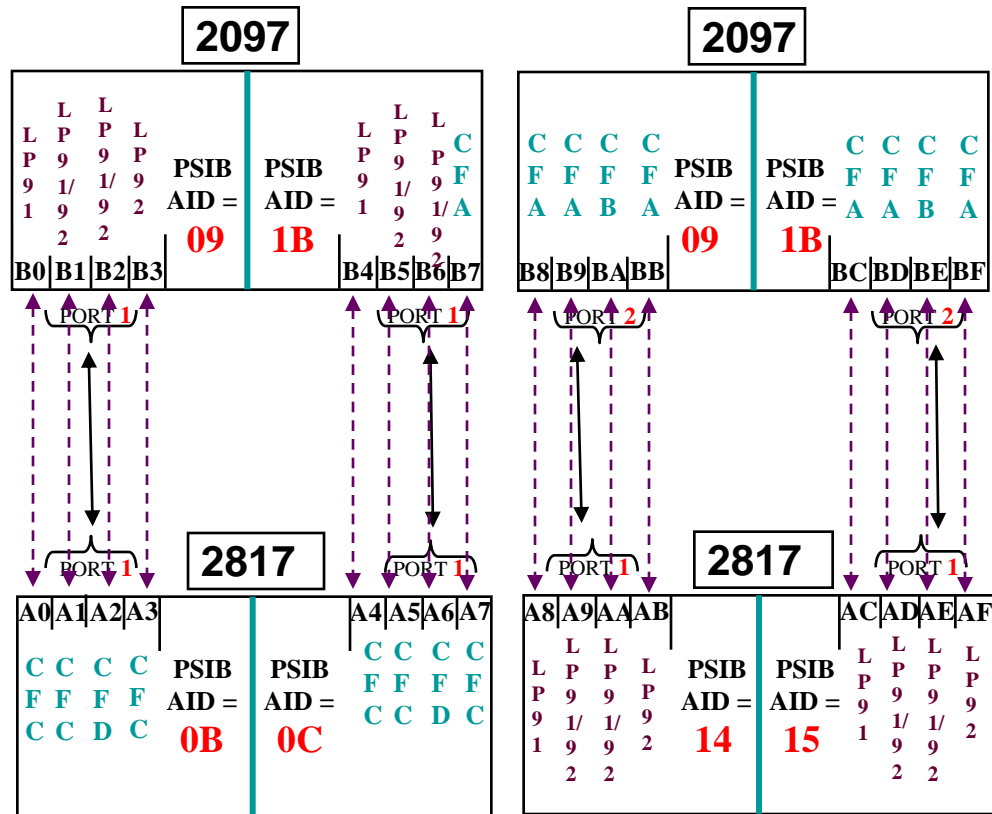


Notes:

- z/OS LPARs may exist on either machine
- CF LPARs
- Z5W has 6 ICF engines
- Z15W has 8 ICF engines

PSIFB LINKS

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ESP - Z5W TO Z15W INFINIBAND CONNECTS



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Z15W ESP INFINIBAND CONNECTS

CPU = **Z-NEXT** (CHP/MODE/LPAR)

AID = 0B 20 Meter <u>PORT 2</u>	AID = 1B 20 Meter <u>PORT 1</u>	AID = 0C 10 Meter <u>PORT 2</u>	AID = 1B 10 Meter <u>PORT 2</u>	AID = 14 20 Meter <u>PORT 2</u>	AID = 1C 20 Meter <u>PORT 1</u>	AID = 15 10 Meter <u>PORT 2</u>	AID = 1C 10 Meter <u>PORT 2</u>
50 S 91	60 D CFC	54 S 91	64 D CFC	58 S 92	68 D CFC	5C S 92	6C D CFC
51 S 91/92	61 D CFC	55 S 91/92	65 D CFC	59 S 91/92	69 S CFC	5D S 91/92	6D D CFC
52 S 91	62 D CFD	56 S 91	66 D CFD	5A S 92	6A D CFD	5E S 91/92	6E S CFD
53 S 91/92	63 D CFD	57 S 91/92	67 D CFD	5B S 91/92	6B D CFD	5F D CFC	6F D CFD
2	1	2	2	2	1	2	2

NOTE: CF LPAR's 'CFC' & 'CFD' ARE IN LCSS 1 (91/92 ARE IN LCSS 0)



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My First Command

```
16:59:57.66 -D XCF,C
16:59:57.67 IXC357I 16.59.57 DISPLAY XCF 333
SYSTEM AE92 DATA

      INTERVAL  OPNOTIFY  MAXMSG  CLEANUP  RETRY  CLASSLEN
          165         168    4096     15      10      956

      SSUM ACTION  SSUM INTERVAL  SSUM LIMIT  WEIGHT  MEMSTALLTIME
          PROMPT                168         N/A        1        NO

      DEFAULT USER INTERVAL:    165
      DERIVED SPIN INTERVAL:    165
      DEFAULT USER OPNOTIFY: +   3

      MAX SUPPORTED CFLEVEL: 16

      MAX SUPPORTED SYSTEM-MANAGED PROCESS LEVEL: 16

      SIMPLEX SYNC/ASYNCH THRESHOLD:    26
      DUPLEX SYNC/ASYNCH THRESHOLD:    26
      SIMPLEX LOCK SYNC/ASYNCH THRESHOLD:    26
      DUPLEX LOCK SYNC/ASYNCH THRESHOLD:    28
```



Z10

IBM z196 zEnterprise

PSIFB
CF and RMFIII

Samples: 1800 Systems: 2 Date: 09/01/09 Time: 09.00.00 Range: 1800 Sec

```

----- Coupling Facility -----
Name      Type  Model Lv1  Dyn  Util% Def Shr Wgt Effect  Rate  Size  Avail
CFIA      2097  E40  16  OFF  23.0  1  0   1.0   18757 20G   17G
CFIB      2097  E40  16  OFF  13.3  1  0   1.0   32894 20G   18G
    
```

```

CF: CFIA
Type  ST System  CF  --- Sync ---  ----- Async -----
Util  Rate  Avg  Rate  Avg  Chng  Del
%      %      Serv  %      %
Structure Name
DSNDBMG_GBP20  CACHE A *ALL  99.5  15467  22  3149  132  0.0  0.0
                CACHE AE91      7544  22  1459  133  0.0  0.0
                CACHE AE92      7923  22  1689  130  0.0  0.0
    
```

```

CF: CFIB
Type  ST System  CF  --- Sync ---  ----- Async -----
Util  Rate  Avg  Rate  Avg  Chng  Del
%      %      Serv  %      %
Structure Name
DSNDBMG_LOCK1  LOCK  A *ALL  92.7  31584  13  135.9  53  0.0  0.0
                LOCK  AE91  14303  13  75.9  53  0.0  0.0
                LOCK  AE92  17281  13  60.0  54  0.0  0.0
    
```

Z10

IBM z196 zEnterprise

PSIFB
CF and RMFIII

Samples: 1800 Systems: 2 Date: 09/01/09 Time: 12.00.00 Range: 1800 Sec

Coupling Facility					Processor					Request	Storage	
Name	Type	Model	Lvl	Dyn	Util%	Def	Shr	Wgt	Effect	Rate	Size	Avail
CFIA	2097	E40	16	OFF	36.1	1	0		1.0	51078	20G	17G
CFIB	2097	E40	16	OFF	0.9	1	0		1.0	926.0	20G	18G

CF: **CFIA**

Structure Name	Type	ST	System	CF Util %	--- Sync ---		----- Async -----			
					Rate	Avg Serv	Rate	Avg Serv	Chng %	Del %
DSNDBMG_GBP20	CACHE	A	*ALL	64.2	15306	22	3287	129	0.0	0.0
	CACHE		AE91		7613	23	1702	127	0.0	0.0
	CACHE		AE92		7694	22	1585	131	0.0	0.0
DSNDBMG_LOCK1	LOCK	A	*ALL	35.1	31689	16	457.4	55	0.0	0.0
	LOCK		AE91		15739	16	246.7	55	0.0	0.0
	LOCK		AE92		15951	16	210.7	55	0.0	0.0



Z10

IBM z196 zEnterprise

PSIFB
CF and RMFIII

```

Samples: 1800      Systems: 2      Date: 09/09/09   Time: 07.30.00   Range: 1800   Sec
----- Coupling Facility -----
Name      Type   Model  Lvl  Dyn  Util%  Def  Shr  Wgt  Effect  Rate    Size  Avail
CFIA      2097   E40    16   OFF  21.6   1    0    1.0  1.0     32639   20G   17G
CFIB      2097   E40    16   OFF  0.6    1    0    1.0  1.0     1033    20G   18G

Samples: 1800      Systems: 2      Date: 09/09/09   Time: 07.30.00   Range: 1800   Sec
CF: CFIA
Type  ST  System  CF  --- Sync ---  ----- Async -----
      Util  Rate  Avg  Rate  Avg  Chng  Del
Structure Name  %      Serv  Serv  %    %
DSNDBMG_GBP20  CACHE A *ALL  62.9  9862  21  1746  171  0.0  0.0
                CACHE AE91  4818  21  890.1  166  0.0  0.0
                CACHE AE92  5044  20  856.2  177  0.0  0.0
DSNDBMG_LOCK1  LOCK  A *ALL  36.0  20542  15  218.8  68  0.0  0.0
                LOCK  AE91  9635  15  114.7  67  0.0  0.0
                LOCK  AE92  10907  14  104.2  68  0.0  0.0
    
```



Z10

IBM z196 zEnterprise

PSIFB CF and RMFIII

Samples: 1800 Systems: 2 Date: 09/09/09 Time: 09.00.00 Range: 1800 Sec

----- Coupling Facility -----				----- Processor -----				Request	- Storage -			
Name	Type	Model	Lvl	Dyn	Util%	Def	Shr	Wgt	Effect	Rate	Size	Avail
CFIA	2097	E40	16	OFF	17.9	1	0		1.0	15019	20G	17G
CFIB	2097	E40	16	OFF	12.0	1	0		1.0	32018	20G	18G

Samples: 1800 Systems: 2 Date: 09/09/09 Time: 09.00.00 Range: 1800 Sec

CF: **CFIA**

Structure Name	Type	ST	System	CF	Util	--- Sync ---		----- Async -----			
						Rate	Avg	Rate	Avg	Chng	Del
					%	Serv		Serv	%	%	
DSNDBMG_GBP20	CACHE	A	*ALL	97.7	12374	20	2271	210	0.0	0.0	
	CACHE		AE91		6166	20	1163	208	0.0	0.0	
	CACHE		AE92		6209	20	1108	213	0.0	0.0	

CF: **CFIB**

Structure Name	Type	ST	System	CF	Util	--- Sync ---		----- Async -----			
						Rate	Avg	Rate	Avg	Chng	Del
					%	Serv		Serv	%	%	
DSNDBMG_LOCK1	LOCK	A	*ALL	92.1	30145	12	72.7	84	0.0	0.0	
	LOCK		AE91		14741	13	39.7	84	0.0	0.0	
	LOCK		AE92		15404	12	33.0	85	0.0	0.0	



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Z10

ICB4
CF and RMFIII

```

Samples: 1200      Systems: 10      Date: 03/12/10      Time: 10.05.00      Range: 1200      Sec
---- Coupling Facility ----- Processor ----- Request - Storage --
Name      Type      Model  Lvl  Dyn  Util%  Def  Shr  Wgt  Effect  Rate      Size  Avail
CFM1      2097      E12   16   OFF  23.8   5    0    4.5  126K   30G      22G
CFM2      2097      E12   16   OFF  16.8   5    0    4.6  71700 30G      21G

Samples: 1200      Systems: 10      Date: 03/12/10      Time: 10.05.00      Range: 1200      Sec
CF: CFM1
Type      ST      System  CF  --- Sync ---      --- Async ---
Structure Name  Util  Rate  Avg  Rate  Avg  Chng  Del
              %              Serv  Rate  Serv  %      %
DSNDB3G_LOCK1  LOCK  A      *ALL  18.2  49925  10   148.5  86   0.0  0.3
              LP80   4606  10   66.2  87   0.0  0.0
              LP81   9248  9    0.6  61   0.4  8.1
              LP83   4962  11   10.0  49   0.6  0.6
              LP85   2285  10   0.4  155  0.0  8.5
              LP86   4666  11   69.9  90   0.0  0.0
              LP87   9634  10   0.4  122  0.4  28.1
              LP88   3109  10   0.4  55   0.8  15.0
              LP89  11416  10   0.6  46   0.6  15.5
DSNDB3G_GBP10  CACHE A      *ALL  6.9   9936  12   514.6  80   0.2  0.2
              LP80  379.6  15   18.0  175  0.0  0.0
              LP81  2377  11   142.0  74   0.0  0.0
              LP83  3295  12   171.5  65   0.4  0.4
              LP85  245.1  12   15.9  95   0.0  0.0
              LP86  357.1  16   13.6  139  0.0  0.0
              LP87  1126  12   49.7  88   0.0  0.0
              LP88  826.5  13   48.4  76   0.2  0.2
              LP89  1330  13   55.5  85   0.1  0.1
DSNDB3G_GBP20  CACHE A      *ALL  12.3  8393  12   1033  84   0.2  0.2
              LP80  317.4  15   23.4  120  0.0  0.0
              LP81  1434  11   278.1  84   0.0  0.0
              LP83  3181  12   238.5  70   0.7  0.7
              LP85  161.9  13   23.5  90   0.0  0.0
              LP86  340.9  14   17.7  126  0.0  0.0
              LP87  1297  13   271.8  96   0.0  0.0
              LP88  418.9  12   51.4  66   0.0  0.0
              LP89  1242  13   128.9  83   0.0  0.0
    
```




IBM z196 zEnterprise

PSIFB CF and RMFIII

Samples: 240 Systems: 2 Date: 08/03/10 Time: 09.23.00 Range: 240 Sec

CF Policy: POLICY6 Activated at: 07/13/10 21.07.08

----- Coupling Facility -----					----- Processor -----					Request	- Storage -	
Name	Type	Model	Lvl	Dyn	Util%	Def	Shr	Wgt	Effect	Rate	Size	Avail
CFC4	2817	M49	17	OFF	0.0	3	0		3.0		9799M	9591M
CFC5	2817	M49	17	OFF	0.0	3	0		3.0		9799M	9591M
CFIA	2097	E40	16	OFF	38.8	3	0		3.0	215K	8098M	4508M
CFIB	2097	E40	16	OFF	1.1	2	0		2.0	1694	8098M	6192M
CFI1	2097	E40	0	N/A	0.0	0	N/A	N/A	0.0		0	0
CFI2	2097	E40	0	N/A	0.0	0	N/A	N/A	0.0		0	0
SEB3	2097	E12	0	N/A	0.0	0	N/A	N/A	0.0		0	0
SEB4	2097	E12	0	N/A	0.0	0	N/A	N/A	0.0		0	0

Samples: 300 Systems: 2 Date: 08/03/10 Time: 10.00.00 Range: 300 Sec

----- Coupling Facility -----					----- Processor -----					Request	- Storage -	
Name	Type	Model	Lvl	Dyn	Util%	Def	Shr	Wgt	Effect	Rate	Size	Avail
CFC4	2817	M49	17	OFF	24.8	3	0		3.0	225K	9799M	8365M
CFC5	2817	M49	17	OFF	0.0	3	0		3.0		9799M	9591M
CFIA	2097	E40	16	OFF	0.4	3	0		3.0	830.1	8098M	5732M
CFIB	2097	E40	16	OFF	1.2	2	0		2.0	2052	8098M	6192M
CFI1	2097	E40	0	N/A	0.0	0	N/A	N/A	0.0		0	0
CFI2	2097	E40	0	N/A	0.0	0	N/A	N/A	0.0		0	0
SEB3	2097	E12	0	N/A	0.0	0	N/A	N/A	0.0		0	0
SEB4	2097	E12	0	N/A	0.0	0	N/A	N/A	0.0		0	0



IBM z196 zEnterprise

z10 CF LPAR Compared to z196 CF LPAR

Samples: 900 Systems: 2 Date: 09/23/10 Time: 09.30.00 Range: 900 Sec

----- Coupling Facility -----					----- Processor -----					Request	- Storage -	
Name	Type	Model	Lvl	Dyn	Util%	Def	Shr	Wgt	Effect	Rate	Size	Avail
CFC4	2817	M49	17	OFF	0.0	3	0		3.0		9799M	9591M
CFC5	2817	M49	17	OFF	0.0	2	0		2.0		9799M	9591M
CFIA	2097	E40	16	OFF	26.4	3	0		3.0	80275	8098M	4420M
CFIB	2097	E40	16	OFF	0.8	2	0		2.0	1438	8098M	6161M

Samples: 900 Systems: 2 Date: 09/23/10 Time: 06.30.00 Range: 900 Sec

----- Coupling Facility -----					----- Processor -----					Request	- Storage -	
Name	Type	Model	Lvl	Dyn	Util%	Def	Shr	Wgt	Effect	Rate	Size	Avail
CFC4	2817	M49	17	OFF	16.4	3	0		3.0	85189	9799M	6005M
CFC5	2817	M49	17	OFF	0.2	2	0		2.0	734.5	9799M	7764M
CFIA	2097	E40	16	OFF	0.0	3	0		3.0		8098M	7994M
CFIB	2097	E40	16	OFF	0.0	2	0		2.0		8098M	7994M

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z10 CF Structure Compared to z196 CF LPAR (1 of 2)

```
Samples: 900      Systems: 2      Date: 09/23/10      Time: 09.30.00      Range: 900      Sec
CF: CFIA          Type  ST System  CF  --- Sync ---      ----- Async -----
                   Util  Rate  Avg  Rate  Avg  Chng  Del
Structure Name     %      Serv
DSNDBMG_GBP20     CACHE A *ALL    31.0 11364 19 2592 190 0.0 0.0
                   AE91    5625 19 1048 199 0.0 0.0
                   AE92    5739 19 1545 184 0.0 0.0
DSNDBMG_GBP21     CACHE A *ALL    21.2 7206 18 2130 167 0.0 0.0
                   AE91    3460 19 1546 150 0.0 0.0
                   AE92    3746 17 583.7 209 0.0 0.0
DSNDBMG_GBP22     CACHE A *ALL    12.4 4661 17 1479 145 0.0 0.0
                   AE91    2299 17 1025 134 0.0 0.0
                   AE92    2362 17 454.5 168 0.0 0.0
DSNDBMG_LOCK1     LOCK  A *ALL    32.7 47623 13 1708 66 0.0 0.0
                   AE91    23946 13 889.1 66 0.0 0.0
                   AE92    23678 13 819.1 66 0.0 0.0
```

IBM z196 zEnterprise

z10 CF Structure Compared to z196 CF LPAR (2 of 2)

```

Samples: 900      Systems: 2      Date: 09/23/10  Time: 06.30.00  Range: 900  Sec
CF: CFC4        Type  ST System  CF  --- Sync ---  ----- Async -----
                Util  Rate  Avg  Rate  Avg  Chng  Del
                %    %    Serv %    %    %    %
Structure Name
DSNDBMG_GBP20  CACHE A  *ALL    27.8  13896  15  2244  164  0.0  0.0
                CACHE  AE91    6962  15  1185  159  0.0  0.0
                CACHE  AE92    6934  16  1059  170  0.0  0.0
DSNDBMG_GBP21  CACHE A  *ALL    20.4  6847  16  2112  136  0.0  0.0
                CACHE  AE91    3506  17  1518  126  0.0  0.0
                CACHE  AE92    3341  15  594.1  162  0.0  0.0
DSNDBMG_GBP22  CACHE A  *ALL    12.6  6094  15  1145  151  0.0  0.0
                CACHE  AE91    3073  15  798.5  136  0.0  0.0
                CACHE  AE92    3021  15  346.4  186  0.0  0.0
DSNDBMG_LOCK1  LOCK  A  *ALL    36.2  50943  11  18.3  62  0.0  0.0
                LOCK  AE91    25240  11  8.1  62  0.0  0.0
                LOCK  AE92    25703  12  10.3  62  0.0  0.0
    
```



IBM z196 zEnterprise

z196
CF High
Utilization

```

Samples: 600      Systems: 2      Date: 09/20/10   Time: 10.24.00   Range: 600      Sec
----- Coupling Facility -----
Name      Type      Model  Lvl  Dyn  Util%  Def  Shr  Wgt  Effect  Rate      Size  Avail
CFC4      2817      M49    17   OFF  38.9   3    0    3.0  361K    9799M    8324M
CFC5      2817      M49    17   OFF  0.0    2    0    2.0  10.4    9799M    9569M
CFIA      2097      E40    16   OFF  2.1    3    0    3.0  4840    8098M    3956M
CFIB      2097      E40    16   OFF  0.0    2    0    2.0           8098M    7994M

CF: CFC4      Type  ST  System  CF  --- Sync ---  --- Async ---
              Util  Rate  Avg  Rate  Avg  Chng  Del
              %    %    %    %    %    %    %
Structure Name
DSNDBMG_GBP20  CACHE A  *ALL    21.3  26540  16  3970  126  0.1  0.1
              CACHE AE91    13353  15  2203  121  0.2  0.2
              CACHE AE92    13188  17  1766  132  0.1  0.1
DSNDBMG_GBP21  CACHE A  *ALL    6.5   5077  19  1328  118  0.1  0.1
              CACHE AE91    2716  21  893.3  110  0.1  0.1
              CACHE AE92    2361  16  434.5  136  0.1  0.1
DSNDBMG_GBP22  CACHE A  *ALL    3.5   3277  18  764.1  107  0.1  0.1
              CACHE AE91    1792  19  495.2  101  0.1  0.1
              CACHE AE92    1484  16  268.9  118  0.1  0.1
DSNDBMG_LOCK1  LOCK  A  *ALL    68.7  317K  11  554.8  51  1.0  5.9
              LOCK  AE91    149K  11  257.5  53  1.3  7.4
              LOCK  AE92    167K  12  297.3  49  0.7  4.6
    
```



IBM z196 zEnterprise

z196 Duplex

This is an example only. Inadequate CF to CF link capacity.

AP - Active Primary

AS - Active Secondary

```

Samples: 300      Systems: 2      Date: 09/21/10   Time: 12.45.00   Range: 300   Sec
----- Coupling Facility -----
Name      Type  Model Lvl  Dyn  Util% Def Shr Wgt Effect  Rate  Size  Avail
CFC4      2817  M49   17   OFF  20.9  3  0   3.0   42875 9799M 8317M
CFC5      2817  M49   17   OFF  23.7  2  0   2.0   32315 9799M 8329M
CFIA      2097  E40   16   OFF  0.7   3  0   3.0    1603 8098M 3897M
CFIB      2097  E40   16   OFF  0.0   2  0   2.0    8098M 7994M

CF: ALL

Type  ST System  CF  --- Sync ---  ----- Async -----
Util  Rate  Avg  Rate  Avg  Chng  Del
%      %      %      %      %      %      %
Structure Name
DSNDBMG_GBP20  CACHE AP *ALL  11.6  6201  16  1222  189  0.0  0.0
                CACHE AE91  2947  15  604.9  187  0.0  0.0
                CACHE AE92  3254  17  617.0  190  0.0  0.0
                CACHE AS *ALL  5.5   0.1  14  1018  148  0.0  0.0
                CACHE AE91  0.1  14  499.6  145  0.0  0.0
                CACHE AE92  0.0  0  518.8  151  0.0  0.0
DSNDBMG_LOCK1 LOCK AP *ALL  76.7  233.6  122  30293  248  0.0  0.0
                LOCK AE91  101.6  135  14610  244  0.0  0.0
                LOCK AE92  132.1  112  15683  252  0.0  0.0
                LOCK AS *ALL  88.6  169.2  163  30285  245  0.0  0.0
                LOCK AE91  81.5  164  14605  241  0.0  0.0
                LOCK AE92  87.6  162  15679  249  0.0  0.0
    
```

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z196 Duplex - constraint relieved

```
Samples: 300      Systems: 2      Date: 09/21/10      Time: 12.55.00      Range: 300      Sec
```

Coupling Facility					Processor					Request		Storage	
Name	Type	Model	Lvl	Dyn	Util%	Def	Shr	Wgt	Effect	Rate	Size	Avail	
CFC4	2817	M49	17	OFF	18.0	3	0		3.0	101K	9799M	8317M	
CFC5	2817	M49	17	OFF	5.0	2	0		2.0	3981	9799M	8819M	
CFIA	2097	E40	16	OFF	1.2	3	0		3.0	2854	8098M	3897M	
CFIB	2097	E40	16	OFF	0.0	2	0		2.0		8098M	7994M	

CF: ALL	Type	ST	System	CF	--- Sync ---	----- Async -----				
Structure Name				Util	Rate	Avg	Rate	Avg	Chng	Del
				%		Serv		Serv	%	%
DSNDBMG_GBP20	CACHE	AP	*ALL	29.3	17269	15	2090	194	0.0	0.0
	CACHE		AE91		8663	15	1093	190	0.0	0.0
	CACHE		AE92		8606	16	997.3	199	0.0	0.0
	CACHE	AS	*ALL	45.9	0.1	12	1929	122	0.0	0.0
	CACHE		AE91		0.1	12	986.3	120	0.0	0.0
	CACHE		AE92		0.0	0	942.3	124	0.0	0.0
DSNDBMG_LOCK1	LOCK	A	*ALL	39.2	63718	11	29.2	62	0.0	0.0
	LOCK		AE91		32187	11	12.5	62	0.0	0.0
	LOCK		AE92		31530	11	16.7	62	0.0	0.0

DB2 software managed Duplex has a relatively low cost

DB2's LOCK structure uses System Managed Duplex, which is expensive.

External CF's reduce the need for Duplexing

Its all about Sync access



IBM z196 zEnterprise

Questions?